

Amendments to the Claims

This listing of claims replaces all prior versions and listing of claims in the application.

1. (CURRENTLY AMENDED) A method of fabrication of a 1T DRAM used in a system which simulates the behavior of a Static Random Access Memory (SRAM), comprising the steps of:

- a) forming a word line structure and a capacitor plate structure on a substrate;
 - (1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;
- b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure;
- c) forming dielectric spacers on the sidewalls of said word line structure and said capacitor plate structure;
- d) forming a mask pattern over said cell node region;
- e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region;
- f) removing the mask pattern;
- g) forming a dielectric layer over said substrate; and
- h) forming a bitline contact to said second bitline region ~~to form a 1T Static Random Access Memory.~~

2. (ORIGINAL) The method of claim 1 wherein said second bit line region preferably has an impurity concentration greater than the cell node region by at least a factor of 10.
3. (ORIGINAL) The method of claim 1 wherein said substrate is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said substrate has an impurity concentration between $1E17$ and $1E18$ atoms/cc.
4. (ORIGINAL) The method of claim 1 wherein said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between $1E17$ and $1E18$ atoms/cc.
5. (ORIGINAL) The method of claim 1 wherein said second bitline region has a concentration between $1E20$ and $1E21$ atom/cc.
6. (ORIGINAL) The method of claim 1 wherein said first bit line region has a p-type doping and has an impurity concentration between $1E18$ and $1E19$ Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between $1E20$ and $1E21$ atoms/cc and said cell node region has a p-type doping and has an impurity concentration between $1E18$ and $1E19$ atom/cc.
7. (ORIGINAL) The method of claim 1 wherein said first bit line region has a p-type doping and has an impurity concentration between $1E18$ and $1E19$ Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between $1E20$ and $1E21$ atoms/cc and said cell node region has a p-type doping and has an impurity concentration between $1E17$ and $1E18$ atom/cc.

8. (CURRENTLY AMENDED) A method of fabrication of a 1T DRAM used in a system which simulates the behavior of a Static Random Access Memory (SRAM), comprising the steps of:

- a) forming a dielectric layer on a substrate; then
forming a conductive layer on said dielectric layer; then
patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;
 - (1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; said capacitor dielectric is comprised of said dielectric layer;
 - (2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between $1E17$ and $1E18$ atoms/cc; then
- b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure; said cell node region and said first bit line region do not intersect;
 - (1) said first bit line region and said cell node region have a p-type doping and have an impurity concentration between $1E18$ and $1E19$ atoms/cc,
- c) forming dielectric spacers on the sidewalls of said word line structure and said capacitor plate structure;
- d) forming a mask pattern over said cell node region;

- e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region; said second bitline region has a concentration between $1E20$ and $1E21$ atom/cc;
- f) removing the mask pattern;
- g) forming a dielectric layer over said substrate; and
- h) forming a bitline contact to said second bitline region to form a 1T DRAM used in a system which simulates the behavior of a Static Random Access Memory.

Claims 9 to 15 (Canceled)

16. **(Currently amended)** A method of fabrication of a 1T DRAM used in a system which simulates the behavior of an Static Random Access Memory (SRAM), comprising the steps of:

- a) forming a dielectric layer on a substrate; said substrate is a silicon wafer; then
- b) forming a conductive layer on said dielectric layer; then
- c) patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;
- (1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; said capacitor dielectric is comprised of said dielectric layer;
- d) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region and said first bit line region do not intersect;

- said first bit line region and said cell node region have a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc; and
- e) forming dielectric spacers on the sidewalls of said word line structure and said capacitor plate structure;
 - f) forming a mask pattern over said cell node region;
 - g) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region;
said second bitline region has a concentration between 1E20 and 1E21 atom/cc;
 - h) removing the mask pattern;
 - i) forming a dielectric layer over said substrate; and
 - j) forming a bitline contact to said second bitline region to form a 1T-DRAM
used in a system which simulates the behavior of a Static Random Access
Memory.

17. (New) The method of claim 1 wherein said substrate is a silicon wafer.

18. (New) The method of claim 8 wherein said substrate is a silicon wafer.